

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74LVX240F, TC74LVX240FT TC74LVX244F, TC74LVX244FT

### Octal Bus Buffer

TC74LVX240 Inverted, 3-State Outputs

TC74LVX244 Non-Inverted, 3-State Outputs

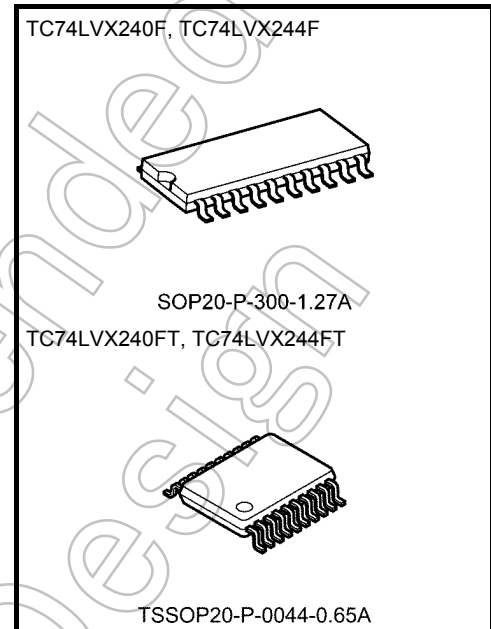
The TC74LVX240,244F/ FT is a high-speed CMOS OCTAL BUS BUFFER fabricated using silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation. This device is suitable for low-voltage and battery operated systems.

The TC74LVX240 is an inverting 3-state buffer while the TC74LVX244 is non-inverting. Both devices have two active-low output enables. These devices are designed to be used in such applications as 3-state memory address drivers.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High-speed:  $t_{pd} = 4.7 \text{ ns (typ.) (VCC = 3.3 V)}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max) (Ta = 25^\circ\text{C})}$
- Input voltage level:  $V_{IL} = 0.8 \text{ V (max) (VCC = 3 V)}$   
 $V_{IH} = 2.0 \text{ V (min) (VCC = 3 V)}$
- Power-down protection provided on all inputs
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Low noise:  $V_{OLP} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74HC240/244

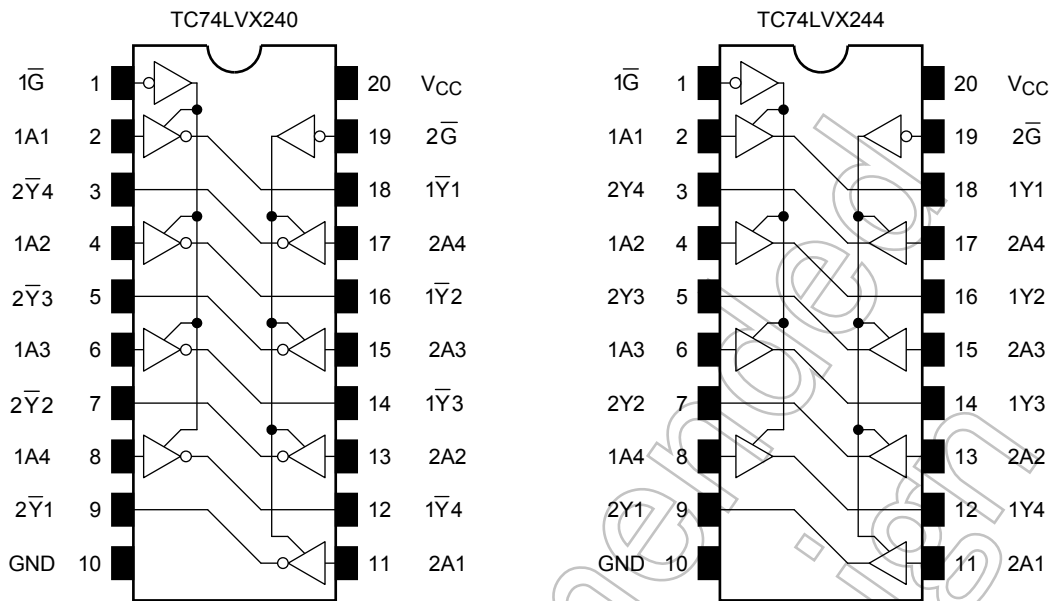


### Weight

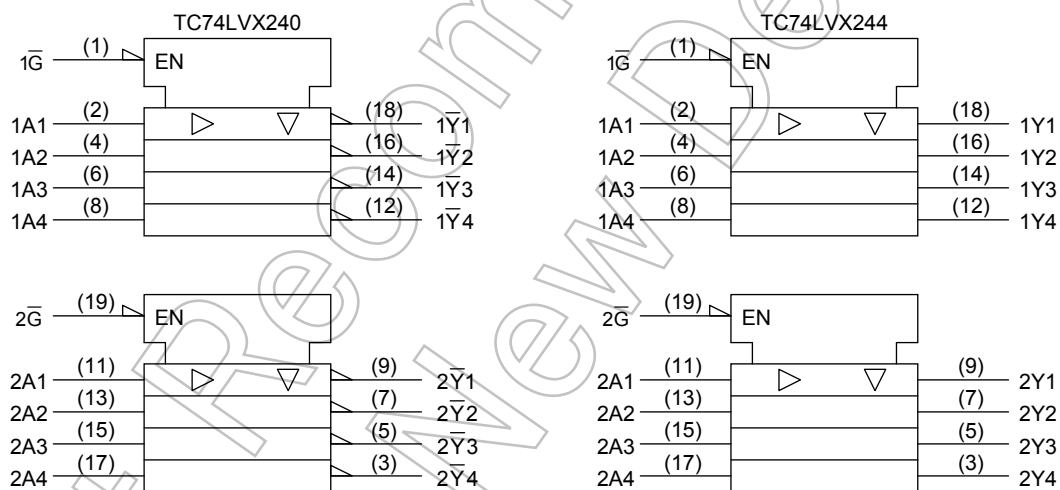
SOP20-P-300-1.27A	: 0.22 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

Start of commercial production  
1993-01

## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

Inputs		Outputs	
$\bar{G}$	$A_n$	$Y_n (244)$	$\bar{Y}_n (240)$
L	L	L	H
L	H	H	L
H	X	Z	Z

X: Don't care

Z: High impedance

**Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 3.6	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	$dt/dv$	0 to 100	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

**Electrical Characteristics**

**DC Characteristics**

Characteristics		Sym- bol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to 85°C		Unit	
					Min	Typ.	Max	Min	Max		
Input voltage	H-level	V <sub>IH</sub>	—	2.0	1.5	—	—	1.5	—	V	
				3.0	2.0	—	—	2.0	—		
				3.6	2.4	—	—	2.4	—		
	L-level	V <sub>IL</sub>	—	2.0	—	—	0.5	—	0.5		
				3.0	—	—	0.8	—	0.8		
				3.6	—	—	0.8	—	0.8		
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				I <sub>OH</sub> = -50 μA	3.0	2.9	3.0	—	2.9	—	
				I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0	0.1	—	0.1	
				I <sub>OL</sub> = 50 μA	3.0	—	0	0.1	—	0.1	
				I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
3-State output Off-state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	3.6	—	—	±0.25	—	±2.5	μA	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	3.6	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	—	—	4.0	—	40.0	μA	

Not Recommended for New Design

## AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max		Min	Max
Propagation delay time (TC74LVX240)	t <sub>pLH</sub>	—	2.7	15	—	5.7	10.1	1.0	12.5	ns
				50	—	8.2	13.6	1.0	16.0	
	t <sub>pHL</sub>		3.3 ± 0.3	15	—	4.3	6.2	1.0	7.5	
				50	—	6.8	9.7	1.0	11.0	
Propagation delay time (TC74LVX244)	t <sub>pLH</sub>	—	2.7	15	—	6.1	11.4	1.0	13.5	ns
				50	—	8.6	14.9	1.0	17.0	
	t <sub>pHL</sub>		3.3 ± 0.3	15	—	4.7	7.1	1.0	8.5	
				50	—	7.2	10.6	1.0	12.0	
Output enable time	t <sub>pZL</sub>	R <sub>L</sub> = 1 kΩ	2.7	15	—	7.1	13.8	1.0	16.5	ns
				50	—	9.6	17.3	1.0	20.0	
	t <sub>pZH</sub>		3.3 ± 0.3	15	—	5.5	8.8	1.0	10.5	
				50	—	8.0	12.3	1.0	14.0	
Output disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1 kΩ	2.7	50	—	11.6	16.0	1.0	19.0	ns
				3.3 ± 0.3	50	—	9.7	11.4	1.0	
Output to output skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
				3.3 ± 0.3	50	—	—	1.5	—	
Input capacitance	C <sub>IN</sub>		(Note 2)		—	4	10	—	10	pF
Output capacitance	C <sub>OUT</sub>		—		—	6	—	—	—	pF
Power dissipation capacitance (Note 3)	C <sub>PD</sub>	TC74LVX240	—		—	17	—	—	—	pF
		TC74LVX244	—		—	19	—	—	—	

Note 1: Parameter guaranteed by design.  
( $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$ )

Note 2: Parameter guaranteed by design.

Note 3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

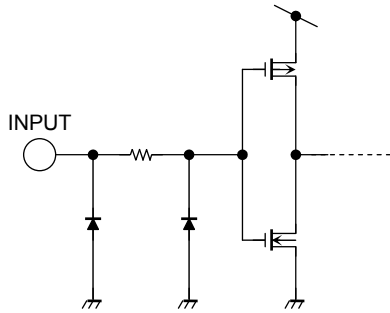
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

**Noise Characteristics (Ta = 25°C, input: tr = tf = 3 ns, CL = 50 pF)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	—	3.3	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	—	3.3	-0.5	-0.8	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	—	3.3	—	0.8	V

**Input Equivalent Circuit**

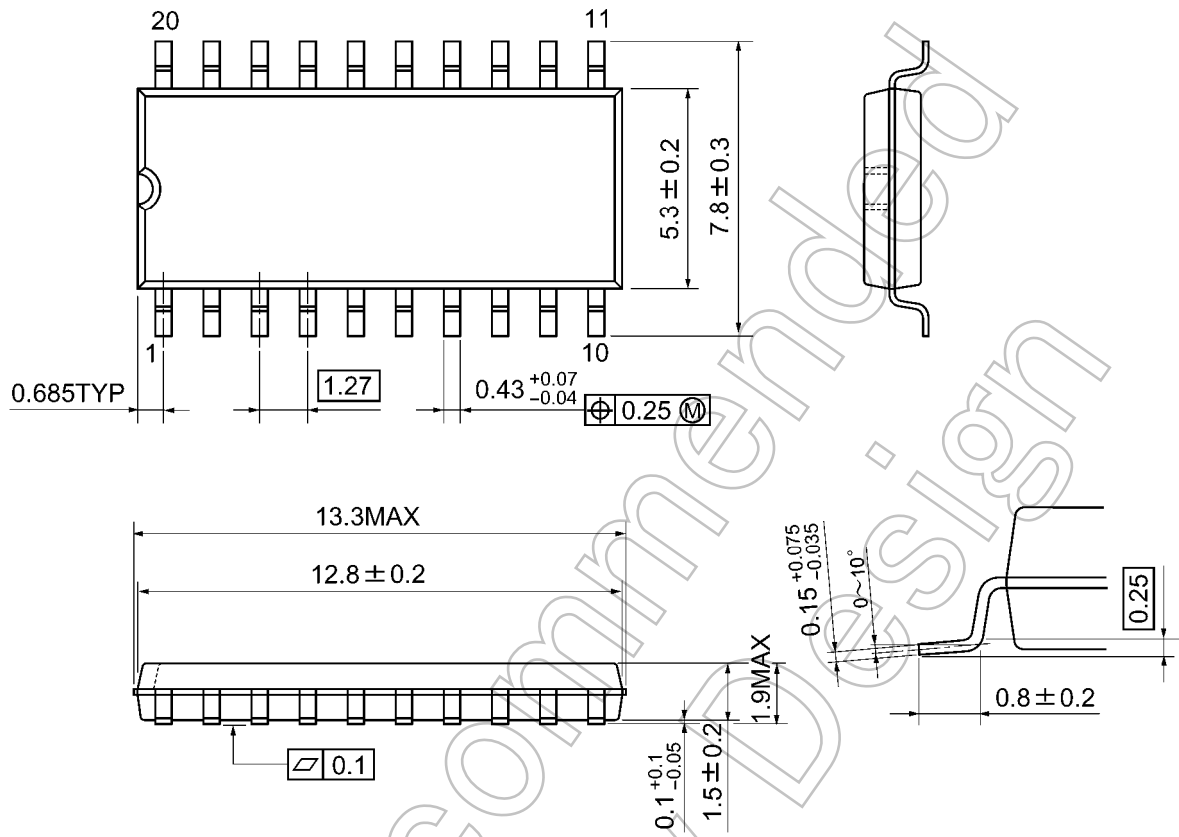


Not Recommended for New Design

**Package Dimensions**

SOP20-P-300-1.27A

Unit: mm



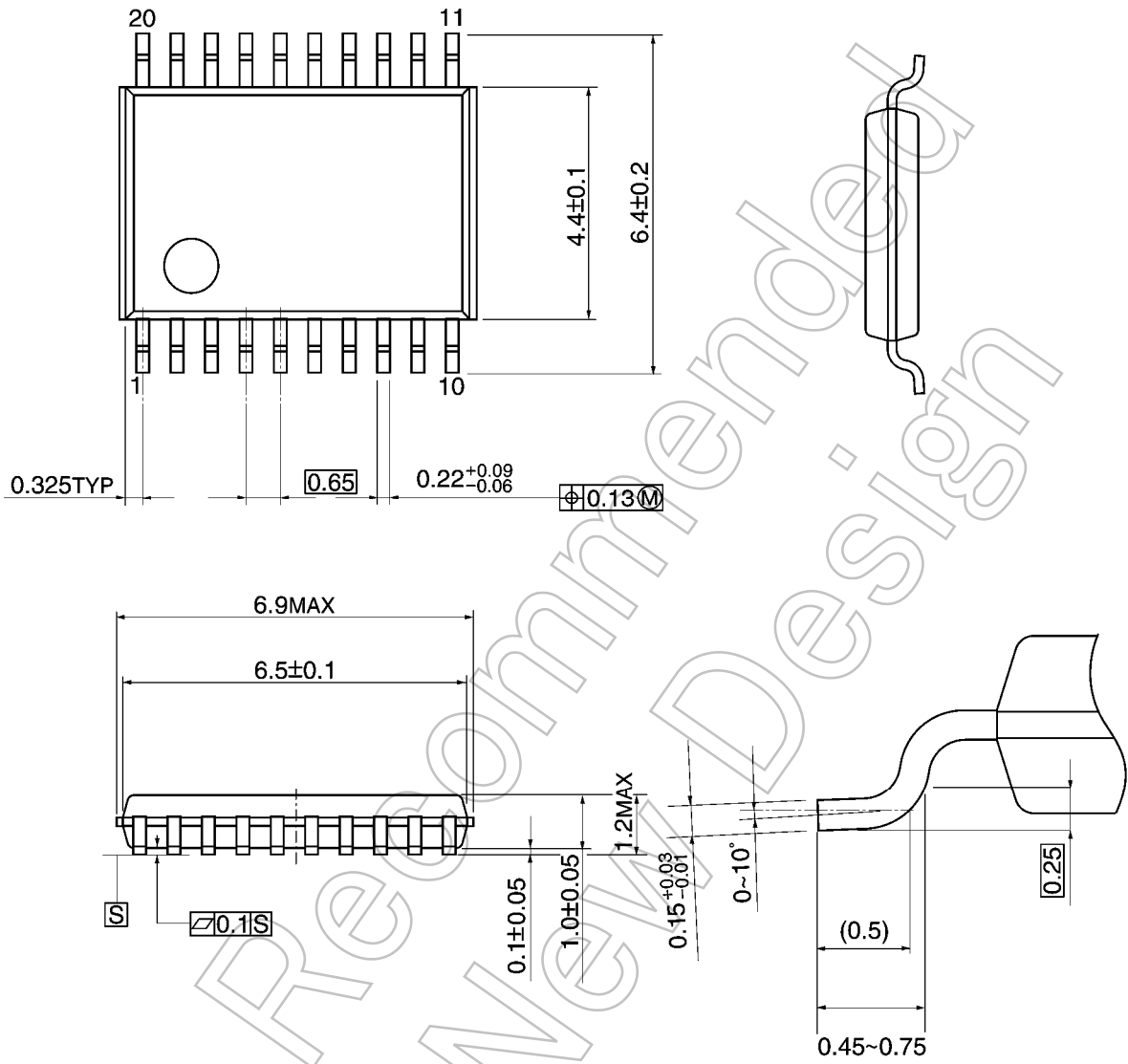
Weight: 0.22 g (typ.)

Not Recommended for New Design

**Package Dimensions**

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

Not Recommended for New Design



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